MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2017/2018SESSION

ECE3226- ADVANCED COMPUTER ARCHITECTURE AND PARALLEL COMPUTING

(CE)

9 MAR 2018
03:00 P.M – 05:00 P.M
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This question paper consists of one (5) pages only (including this page).
2. There are **FOUR (4) QUESTIONS** in this paper. Answer **ALL QUESTIONS**. All questions carry 25 marks each.
3. Write your answers in the Answer Booklet provided.

Question 1

a) What is it meant by SIMD? Elaborate the general characteristics of SIMD computers and draw a simple sketch of SIMD architecture.

[7 marks]

b) As a microprocessor architect, you can designa microprocessor based on 2 categories of memory systems. Name the two memory categories and elaborate the definition of categories in your own words.

[4 marks]

c) Direct Memory Access is a feature of computer systems that allows certain hardware subsystems to access main system memory, independent of the central processing unit. Specify three types of DMA transfer techniques.

[3 marks]

d) Table 1 shows an execution mix and run times for two computer systems, System A and System C. Table 2 shows run times for System A with different execution mix.

i. Calculate the weighted average time for System A in Table 1 and Table 2.

[4 marks]

ii. Calculate the weighted average time for System C in Table 1.

[2 marks]

iii. Using execution mix in Table 1, find out whether System A or System C is faster, show your results in percentage in terms of how much percentage faster.

[2.5 marks]

iv. Using the new execution mix in Table 2, find out whether System A or System C is faster, show your results in percentage in terms of how much percentage faster.

[2.5 marks]

Program	Execution Frequency	System A Execution Time	System C Execution Time
V	50%	50	500
W	30%	200	600
X	10%	250	500
Y	5%	400	800
Z	5%	5000	3500

Table 1: The execution mix for 5 programs on 2 systems and the weighted average of the running times.

Program	System A Execution Time	System A Execution Frequency
V	50	25%
W	200	5%
X	250	10%
Y	400	5%
Z	5000	55%

Table 2: The weighted average running times for system A using a revised execution mix.

Continued .....

Question 2

a) The DLX design is widely used as fundamental computer architecture for engineers to get knowledge about RISC processor in terms of instruction encoding and decoding.

i. List down the FOUR classes of instructions used in the operations of DLX architecture and explain them in your own words.

[5 marks]

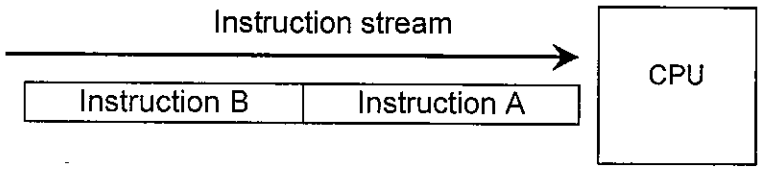
ii. Show the FIVE phases of DLX operations.

[5 marks]

b) State the available hazards which prevents next instruction from executing during the designated clock cycle. Explain and elaborate each of the hazards.

[6 marks]

c) There are 3 types of data hazards, which can be classified based on the order of read and write accesses in the instructions. Name the three types of data hazard and illustrate them by consider two instructions, A and B. A occurs before B.



[9 marks]

Continued .....

Question 3

a) Vector processors can greatly improve performance on certain workloads. As an engineer, define the term of vector, vector processing and vectorizer.

[6 marks]

b) Vector processors are the technology used in modern computers and central processing units because many performance optimization methodologies are applied in them. List out FOUR properties of vector processing.

[6 marks]

c) Show the following code sequence lays out in convoys, assuming a single copy of each vector functional unit:

```
LV      V1,Rx     ;load vector X
MULVS.D V2,V1,F0  ;vector-scalar multiply
LV      V3,Ry     ;load vector Y
ADDVV.D V4,V2,V3  ;add two vectors
SV      V4,Ry     ;store the sum
```

[4 marks]

i) Estimate the number of chimes that will be taken by this vector sequence.

[1 mark]

ii) Calculate the number of cycles per FLOP (floating-point operation), assumptions are made by ignoring the vector instruction issue overhead.

[2 marks]

d) A bank busy time is estimated to be 6 clock cycles and a total memory latency is estimated to be 12 cycles, if we are given 8 memory banks:

i) Calculate the number of clock cycles required to complete a 64 element vector load with a stride of 1?

[3 marks]

ii) Estimate the number of clock cycles required to complete a 64 element vector load with a stride of 32?

[3 marks]

Continued .....

Question 4

a) Hyper Threading is a proprietary simultaneous multithreading (SMT) implementation used to improve parallelization of computations and a multi-core processor is a single computing component with two or more independent processing units. List down any FOUR differences between multi-core architecture and hyper-threading technology.

[8 marks]

b) The Amdahl's Law inequality is sometimes treated as a performance model, instead of a performance limit, list down THREE problems faced by Amdahl's law in parallel computer?

[6 marks]

d) Derive a data-flow graph for the if-else statement below.

```
if( i < 50 )
{
        j = ( i - 12 ) / 6;
}
else
{
        j = ( i + 6 ) / 6 ;
}
```

[5 marks]

d) Very long instruction word (VLIW) refers to instruction set architectures designed to exploit instruction level parallelism (ILP). VLIW machines behave much like superscalar machines with THREE differences. List down the differences.

[6 marks]

End of Paper